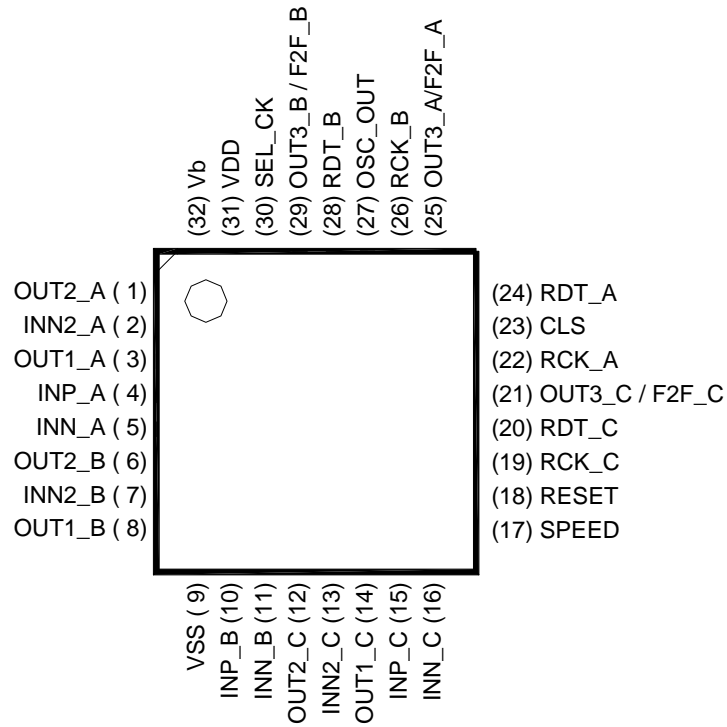


AIS-2103N

Triple Channel F2F Decoder ASIC

Doc. AIS-210x_v2_0.doc





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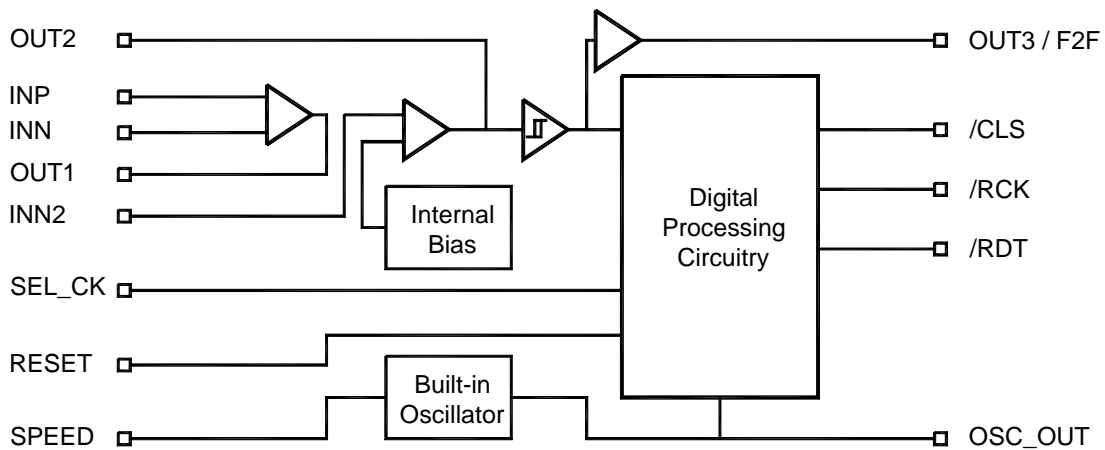
Introduction

The F2F Decoder Integrated Circuit is used to recover F2F encoded data received from a magnetic head. It is commonly used in Point-of-Sales terminal and electronic money transfer terminal.

Basic Features

- >> 0.6um CMOS ASIC IC for F2F magnetic stripe card reader
- >> Built-in operational amplification circuitry, oscillator and digital circuitry
- >> Low power operation
- >> Full operation from 3.0 to 5.5V
- >> Support for both 75/210 BPI recording density
- >> Speed range: 10 ~ 150 cm/s for 75 BPI (Track #2)
10 ~ 100 cm/s for 210 BPI (Track #1/3)
- >> Selectable strobe period for 6 ~ 15us to 1/4 of period for different MCU triggering model
- >> F2F output is available to handle for non standard magnetic stripe
- >> Triple Channel Small Outline Quad Package, 32 pin QFN SMD
- >> Typical Current: 4.0 mA at 5.0V

Block Diagram of F2F Decoder



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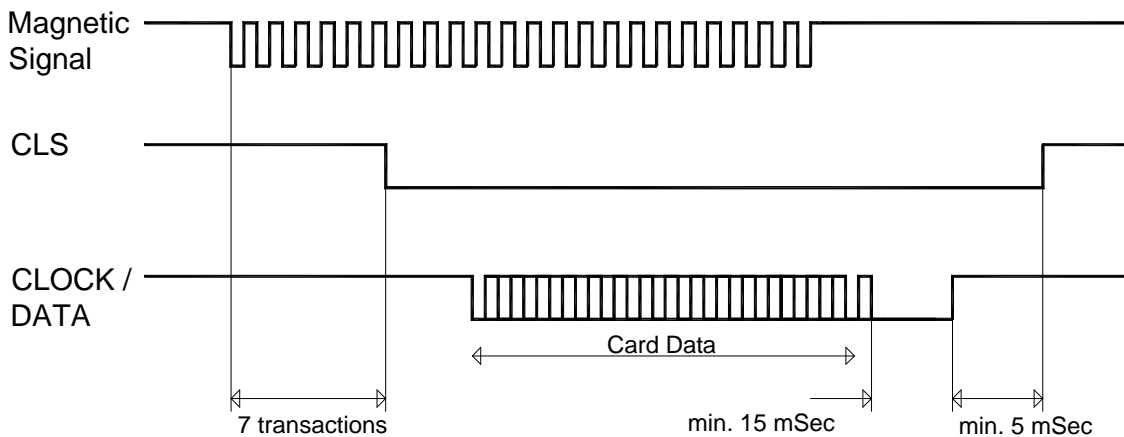


Functional Description

The integrated circuit is an interface for magnetic stripe reader. Magnetic head is connected to the INN and INP terminals. When a magnetic stripe pass over the magnetic head, the encoded analog F2F signal is amplified, filtered and decoded to generate digital signals for DATA (RDT), CLOCK (RCK) and CARD LOAD SIGNAL (CLS). These digital signals are compliant to traditional magnetic stripe reader circuits and can be directly connected to most of micro-controllers.

Timing Diagram of CLS

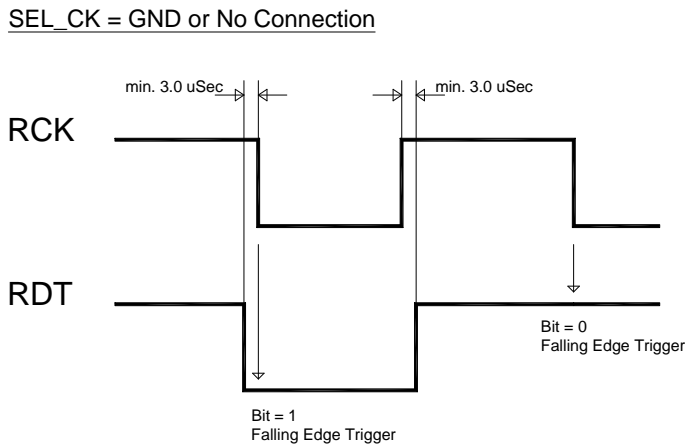
Card Load Signal will go low during card present. CLS will return to normal state after analog signal disappears. It uses to wake up micro-controller which reverts from sleep mode in old day. As micro-controller is running very fast and low power today, it is not necessary to use this terminal. Let it open in normal use.





Timing Diagram of RCK

RCK indicates when data is valid in the RDT. It is recommended that RDT should be read on the falling edge of RCK signal.

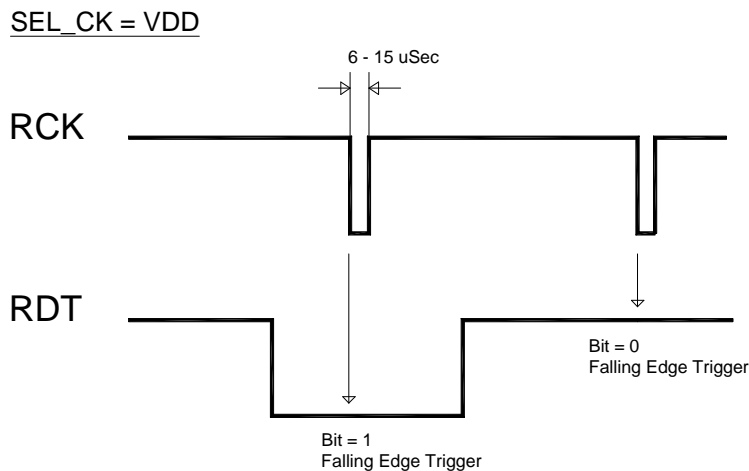


Timing Diagram of RDT

RDT is valid in the falling edge of RCK. If the RDT signal is high, the bit is a ZERO. If the RDT signal is low, the bit is an ONE.

Timing Diagram of SEL_CK

When this pin is level high, RCK has fixed width 6 ~ 15us. When it is level low, RCK has $\frac{1}{4}$ of the period. This pin is internal pull low.



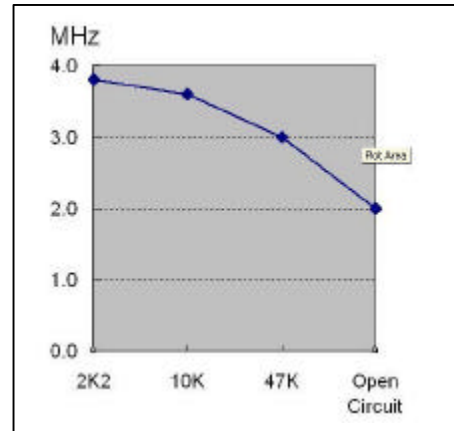
Function of RESET

RESET pin is used to reset the digital decoding logic in the F2F decoder. In normal operation, it will reset itself after each read cycle. No Connection in normal use.



Function of SPEED

SPEED terminal uses to control the operating frequency of decoder's logic section. With a resistor connected from VDD to SPEED terminal, operating frequency will increase. It uses to handle non-standard F2F stream. Let this terminal open circuit in normal operation.



Function of OSC_OUT

Output of the internal oscillator. Let this terminal open circuit in normal operation.

Function of OUT3/F2F

OUT3/F2F pin is the output of the un-decoded magnetic stripe signal. Let this terminal open in normal operation

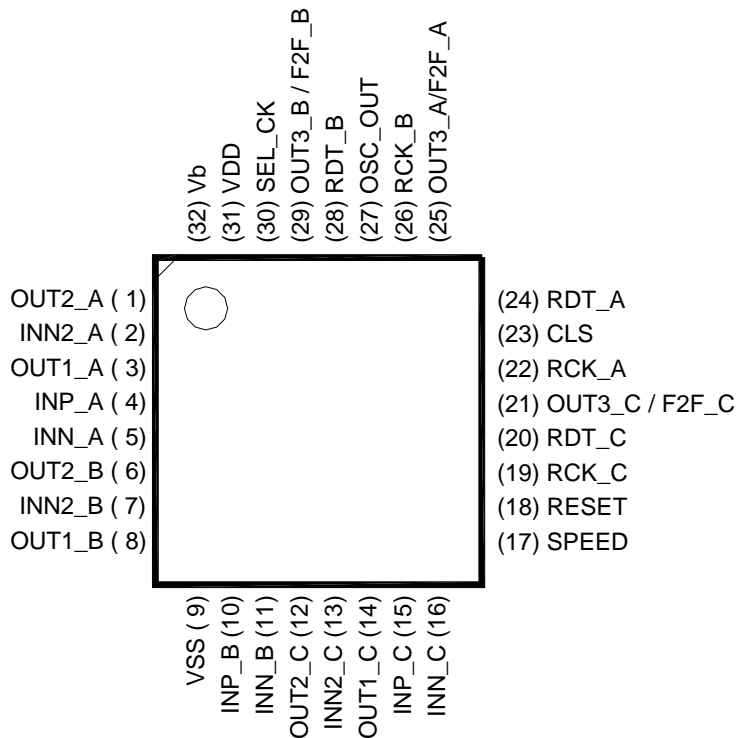


Pin Assignment and Recommended Circuit

AIS-2103N, Triple Channel F2F Decoder in QFN

Pin	Characteristics	Function
1	Internal use	OUT2_A
2	Internal use	INN2_A
3	Internal use	OUT1_A
4	Analog Input	INP_A
5	Analog Input	INN_A
6	Internal use	OUT2_B
7	Internal use	INN2_B
8	Internal use	OUT1_B
9	Power	VSS
10	Analog Input	INP_B
11	Analog Input	INN_B
12	Internal use	OUT2_C
13	Internal use	INN2_C
14	Internal use	OUT1_C
15	Analog Input	INP_C
16	Analog Input	INN_C

Pin	Characteristics	Function
17	Analog Input	SPEED
18	Digital Input	RESET
19	Digital Output	RCK_C
20	Digital Output	RDT_C
21	Digital Output	OUT3_C / F2F_C
22	Digital Output	RCK_A
23	Digital Output	CLS
24	Digital Output	RDT_A
25	Digital Output	OUT3_A / F2F_A
26	Digital Output	RCK_B
27	Digital Output	OSC_OUT
28	Digital Output	RDT_B
29	Digital Output	OUT3_B / F2F_B
30	Digital Input	SEL_CK
31	Power	VDD
32	Analog Input	Vb



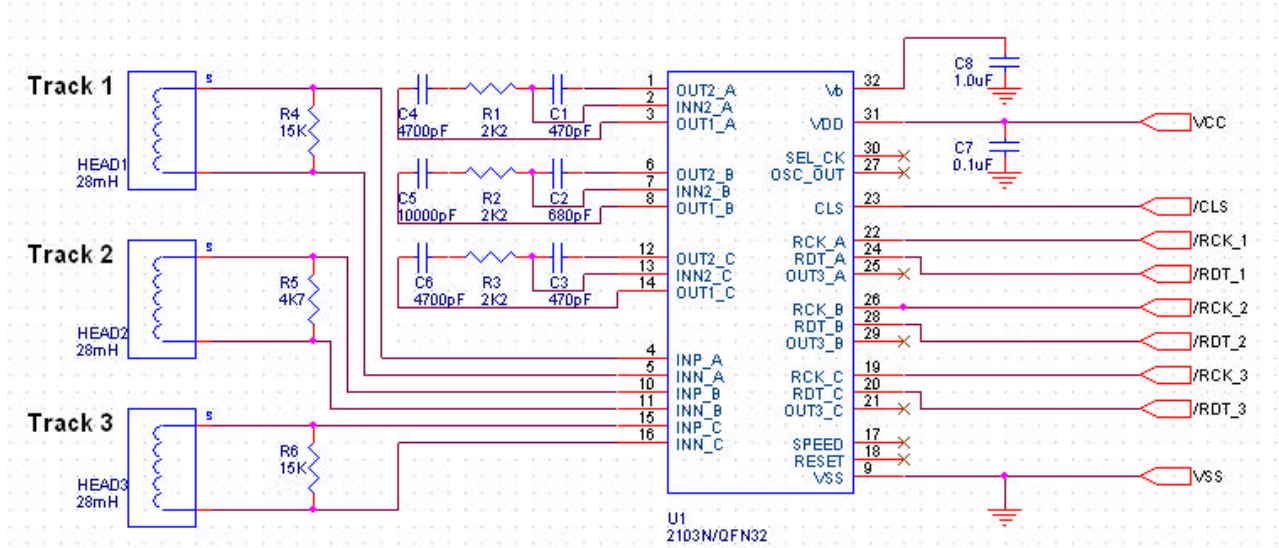
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Recommended Circuit (AIS-2103N)

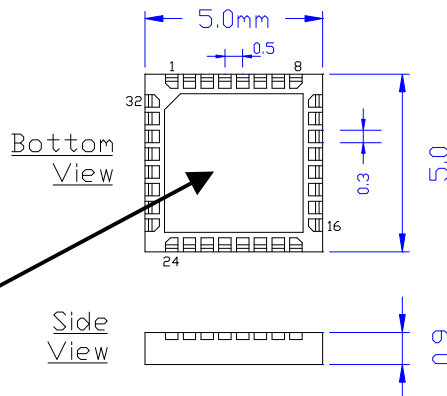


Magnetic Head:
Inductance: 28mH

RC Circuit:
Track 1: C1 / C4 / R1 : 470pF / 4700pF / 2K2
Track 2: C2 / C5 / R2 : 680pF / 10,000pF / 2K2
Track 3: C3 / C6 / R3 : 470pF / 4700pF / 2K2

Magnetic Head Output Circuit:
Track 1: R4: 15K
Track 2: R5: 4K7
Track 3: R6: 15K

Physical Dimensions



Bottom pad should be soldered to ground

Part No.: AIS-2103N
Package: QFN 32 (MO-220)

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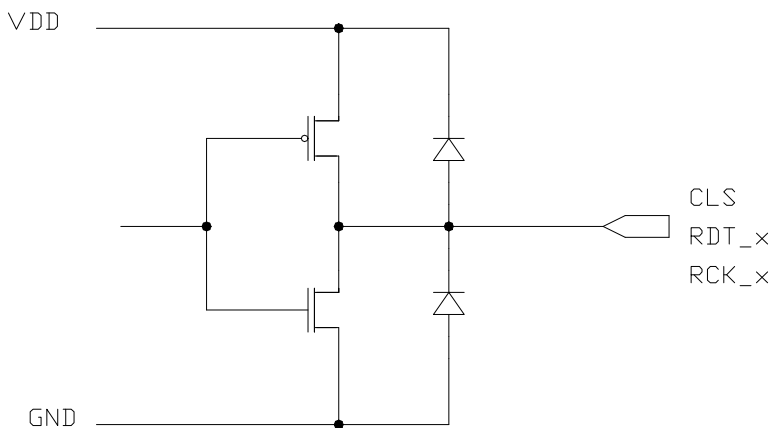
Electrical Parameters

DC Characteristics

Test Condition: VDD=5.0 Volt. Temperature=25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Operating Voltage (V _{DD})	*	3.0		5.5	V
Device Current (I _D)			4.0		mA
Logic Low Output (V _{OL})	At 4mA			0.4	V
Logic High Output (V _{OH})	At 4mA	3.5			V
Oscillator Frequency (F _{osc})			2000		KHz
Operating Temperature		0		55	°C

Equivalent Model of Digital Output



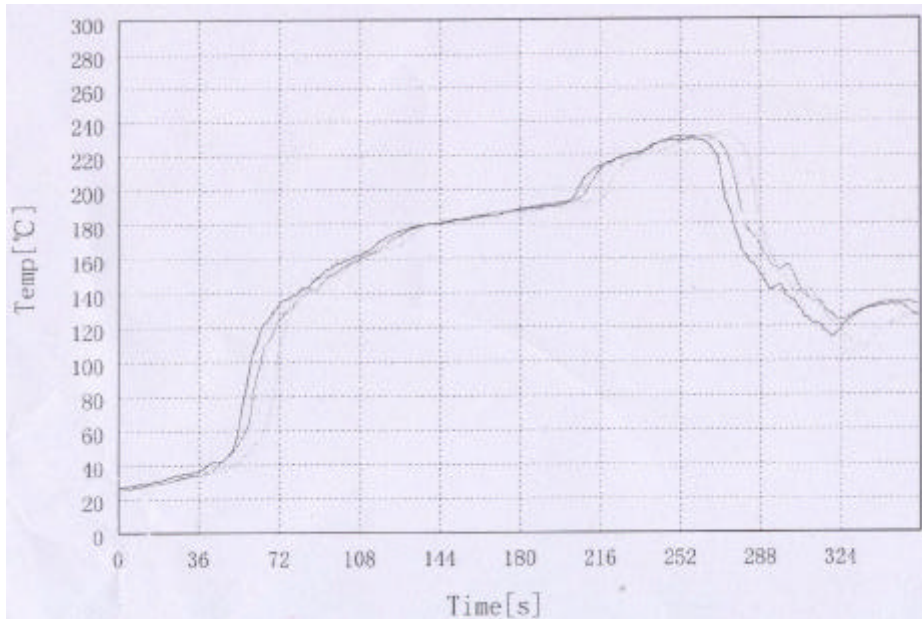
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Recommended Soldering Temperature Profile



Profile Feature	Sn-Pb Assembly	Pb-Free Assembly
Average ramp-up rate	3°C/Sec max 217°C to peak	3°C/Sec max 217°C to peak
Preheat temperature	125 (±25)°C	175 (±25)°C
Preheat time	60 – 120	60 – 180
Time maintained above	183°C 60 – 150	217°C 60 – 150
Peak temperature range	240(+0/-5)°C	260(+0/-5)°C
Time within 5°C of actual peak temperature	10 – 30 sec	20 – 40 sec
Ramp-down rate	6°C/Sec max	6°C/Sec max
Time 25°C to peak temperature	6 minutes maximum	8 minutes maximum

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Data Reading from Magnetic Card

On magnetic card, the encoded data are enclosed by “start sentinel” and “end sentinel”. The detail of the sentinel and data format, please refer to next table. There are leading zeros on the card that used to synchronize the clock frequency and the reading speed. After the leading zeros, the “start sentinel”, “encoded data”, “end sentinel”, “LRC”. Trailing zeros filled the remain section of the card.

<<0000...00>> <<Start Sentinel>> <<Data0>> <<Data1>> <<.....>> <<End Sentinel>> <<LRC>> <<00000...000>>

<<Data>> = << b0><b1><b2><b3><P>> for Track 2 / 3

<<Data>> = << b0><b1><b2><b3><b4><b5><P>> for Track 1

<<LRC>> = Exclusive OR of all characters including the start sentinel and stop sentinel.

For Track 2 and 3, there are 4 bits and an odd parity bit for each character. So that it represents numeric only.

On Track 2, the data characters, control characters, start and end sentinels, and longitudinal redundancy check character shall together not exceed 40 characters.

On Track 3, all characters together shall together not exceed 107 characters.

On Track 1, there are encoded with ASCII code, the total characters shall not exceed 79 characters.

Track #2 / 3 Encoded Data Format

Char	Binary							Char	Binary						
	P			3	2	1	0		P			3	2	1	0
0	1			0	0	0	0	8	0			1	0	0	0
1	0			0	0	0	1	9	1			1	0	0	1
2	0			0	0	1	0	:	1			1	0	1	0
3	1			0	0	1	1	;	0			1	0	1	1
4	0			0	1	0	0	<	1			1	1	0	0
5	1			0	1	0	1	=	0			1	1	0	1
6	1			0	1	1	0	>	0			1	1	1	0
7	0			0	1	1	1	?	1			1	1	1	1

;	Start Sentinel	=	Field Separator	?	End Sentinel
---	----------------	---	-----------------	---	--------------



Track #1 Encoded Data Format

Char	Binary							Char	Binary						
	P	5	4	3	2	1	0		P	5	4	3	2	1	0
Space	1	0	0	0	0	0	0	@	0	1	0	0	0	0	0
!	0	0	0	0	0	0	1	A	1	1	0	0	0	0	1
"	0	0	0	0	0	1	0	B	1	1	0	0	0	1	0
#	1	0	0	0	0	1	1	C	0	1	0	0	0	1	1
\$	0	0	0	0	1	0	0	D	1	1	0	0	1	0	0
%	1	0	0	0	1	0	1	E	0	1	0	0	1	0	1
&	1	0	0	0	1	1	0	F	0	1	0	0	1	1	0
'	0	0	0	0	1	1	1	G	1	1	0	0	1	1	1
(0	0	0	1	0	0	0	H	1	1	0	1	0	0	0
)	1	0	0	1	0	0	1	I	0	1	0	1	0	0	1
*	1	0	0	1	0	1	0	J	0	1	0	1	0	1	0
+	0	0	0	1	0	1	1	K	1	1	0	1	0	1	1
,	1	0	0	1	1	0	0	L	0	1	0	1	1	0	0
-	0	0	0	1	1	0	1	M	1	1	0	1	1	0	1
.	0	0	0	1	1	1	0	N	1	1	0	1	1	1	0
/	1	0	0	1	1	1	1	O	0	1	0	1	1	1	1
0	0	0	1	0	0	0	0	P	1	1	1	0	0	0	0
1	1	0	1	0	0	0	1	Q	0	1	1	0	0	0	1
2	1	0	1	0	0	1	0	R	0	1	1	0	0	1	0
3	0	0	1	0	0	1	1	S	1	1	1	0	0	1	1
4	1	0	1	0	1	0	0	T	0	1	1	0	1	0	0
5	0	0	1	0	1	0	1	U	1	1	1	0	1	0	1
6	0	0	1	0	1	1	0	V	1	1	1	0	1	1	0
7	1	0	1	0	1	1	1	W	0	1	1	0	1	1	1
8	1	0	1	1	0	0	0	X	0	1	1	1	0	0	0
9	0	0	1	1	0	0	1	Y	1	1	1	1	0	0	1
:	0	0	1	1	0	1	0	Z	1	1	1	1	0	1	0
;	1	0	1	1	0	1	1	[0	1	1	1	0	1	1
<	0	0	1	1	1	0	0	\	1	1	1	1	1	0	0
=	1	0	1	1	1	0	1]	0	1	1	1	1	0	1
>	1	0	1	1	1	1	0	^	0	1	1	1	1	1	0
?	0	0	1	1	1	1	1	_	1	1	1	1	1	1	1

%	Start Sentinel	^	Field Separator	?	End Sentinel
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Ordering Information

Part Number	Description	Package
AIS-2103N	Triple Channel F2F Decoder for MSR RoHS Compliant	QFN32

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